LOAN DOCUMENT

DTIC ACCESSION NUMBER

LEVEL

INVENTORY

DOCUMENT IDENTIFICATION

DISTRIBUTION STATEMENT

**H
A
N
D
L
E**

**W
I
T
H**

**C
A
R
E**

ACCESSION FOR

NTIS	GRA&I
DTIC	TRAC
UNANNOUNCED	
JUSTIFICATION	

BY

DISTRIBUTION/

AVAILABILITY CODES

DISTRIBUTION	AVAILABILITY AND/OR SPECIAL
A-1	

DISTRIBUTION STAMP

**Reproduced From
Best Available Copy**

DATE ACCESSIONED

DATE RETURNED

19981223 021

DATE RECEIVED IN DTIC

REGISTERED OR CERTIFIED NUMBER

PHOTOGRAPH THIS SHEET AND RETURN TO DTIC-FDAC

DTIC FORM 70A JUN 90   DOCUMENT PROCESSING SHEET   PREVIOUS EDITIONS MAY BE USED UNTIL STOCK IS EXHAUSTED.
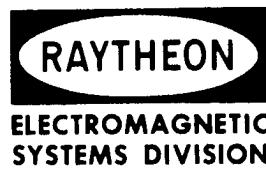
LOAN DOCUMENT

NO DISTRIBUTION
STATMENT

NADC

Tech. Info.

APPENDIX 35

TEST PROCEDURE FOR SYSTEM CONTROLLER

FINAL SOFTWARE REPORT

DATA ITEM NO. A005

INTEGRATED ELECTRONIC WARFARE SYSTEM
ADVANCED DEVELOPMENT MODEL (ADM)

PREPARED FOR:

NAVAL AIR DEVELOPMENT CENTER
WARMINSTER, PENNSYLVANIA

CONTRACT N62269-75-C-0070

RAYTHEON

ELECTROMAGNETIC
SYSTEMS DIVISION

1 OCTOBER 1977

APPENDIX 35

TEST PROCEDURE FOR SYSTEM CONTROLLER

FINAL SOFTWARE REPORT

DATA ITEM A005

INTEGRATED ELECTRONIC WARFARE SYSTEM (IEWS)
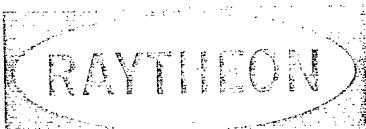ADVANCED DEVELOPMENT MODEL (ADM)

Contract No. N62269-75-C-0070

Prepared for:

Naval Air Development Center
Warminister, Pennsylvania

Prepared by:

RAYTHEON COMPANY
Electromagnetic Systems Division
6380 Hollister Avenue
Goleta, California 93017

1 OCTOBER 1977

TYPE OF SPEC

Software Test Specification

TITLE OF SPEC

Test Procedure for System Controller, IEWS.

FUNCTION	APPROVED	DATE	FUNCTION	APPROVED	DATE
WRITER	D.B. Eldridge	9/21/76			

REVISIONS

CHK	DESCRIPTION	REV	CHK	DESCRIPTION	REV

REVISION																								
SHEET NO.																								
REV STATUS OF SHEETS	REVISION																							
	SHEET NO.																							

PREPRODUCTION TEST PROCEDURE

PART I

PERFORMANCE TEST UNDER LABORATORY CONDITIONS

FOR

SYSTEM CONTROLLER, IEWS

CONTRACT-N62269-74-C-0070

MANUFACTURER--RAYTHEON COMPANY

Total Pages in the Procedure: 27

TABLE OF TESTS

LIST OF TEST EQUIPMENT

1. Local Control Panel (854952-1) and Control Panel Interface Module (894629-4)

2. 4K PROM/RAM Module (950026-4)

3. Signal Sorter (893651)

4. Auxiliary Bus Monitor

5. Simulated System Controller or Software Development Center

6. Test Function Unit (see Appendix A)

Cables (see Appendix A)

a. Signal Sorter Bus Cable

b. Auxiliary Bus Cable

c. Daisy Chain Bus Cables (2)

d. Serial IØ Bus Cable

e. Power Cable

See Appendix A for basic test equipment configuration.

A number of programs are required to facilitate system testing. Some are contained as firmware in the 4K PROM/RAM module. Others are software programs which must be loaded into a two-port 4K RAM memory in the Simulated System Controller or Software Development Center as called out in the test procedure. A list of test programs and associated document control numbers are contained in Appendix B.

Tests in some sections require the use of a MOVE utility program, located on the 4K PROM/RAM, to relocate programs from 4K memory sectors on the Master Bus to 4K sectors on the Slave Buses. A description of the use of this program is contained in Appendix C.

Some tests require the operator to use the SSC or SDC to load external software into the 4K SSC or SDC memory accessible to the SC. A description of this load procedure is contained in Appendix D. Use of the MOVE utility program contained in the 4K PROM/RAM is also required.

LIST OF ABBREVIATIONS

AUX BUS	AUXILIARY BUS
CPI	CONTROL PANEL INTERFACE MODULE
DSIØ	DUAL CHANNEL SERIAL IØ MODULE
LCP	LOCAL CONTROL PANEL
LD/LR	LINE DRIVER/LINE RECEIVER MODULE
PIN/RTC	PRIORITY INTERRUPT NETWORK/REAL TIME CLOCK MODULE
SC	SYSTEM CONTROLLER
SCM	SYSTEM CONTROL MODULE
SDC	SOFTWARE DEVELOPMENT CENTER
SIØ	SERIAL IØ CHANNEL
SS	SIGNAL SORTER
SSC	SIMULATED SYSTEM CONTROLLER
TFU	TEST FUNCTION UNIT

1. GENERAL – Unless specified otherwise, all tests shall be performed under the following conditions:

   (a) Atmospheric Conditions – The tests shall be performed at prevailing open environment atmospheric conditions.

   (b) Input Power – The input power shall be 115 volt, 400 Hertz, three phase.

   (c) Configuration – Unless otherwise specified, all tests shall be performed using the basic test configuration of Appendix A, with power applied to all units.

   (d) Equipment Operation – The test operator shall have familiarity with the operation of both the test equipment and the unit under test.

2. UNIT TEST – Apply power to the basic configuration and momentarily depress the RESET pushbutton on the SC front panel

2.1 OPERATOR CONTROL

2.1.1 Front Panel Reset

   (a) Requirement – Front Panel Reset shall initialize SC, SS and externally cabled SIØ and Daisy Chain devices.

   (b) Conditions – Basic test configuration.

   (c) Measurement – Depress Front Panel RESET pushbutton. Test Function Unit lights SIØCLR and DCMCL should be on. RUN light on LCP should be off.

   _____
   Initial

2.1.2 Local Control Panel

   (a) Requirement – LCP functions shall be fully operational.

   (b) Conditions – Basic test configuration.

   (c) Measurement –

      i. Exercise LCLR function. Test Function unit lights SIØCLR and DCMCL should be on when LCP EXECUTE pushbutton is depressed.

   _____
   Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

I-5

ii. Exercise PCLR function as in (i).
    Lights should remain off.

                                    _____
                                      Initial

iii. Exercise REGSEL function. Load the
     following hexadecimal patterns into
     the data registers and verify upon
     load completion that the contents of
     each register is unchanged.

                    SR   5555

                    PR   3333

                    BR   0F0F

                    XR   00FF

                    ACR AAAA

                    ER   CCCC

                    WR   F0F0

                    AR   FF00   _____
                                     Initial
     Load the following patterns into each
     data register(SR,PR,BR,XR,ACR,ER,WR,AR).

                    0000

                    FFFF

                    5555

                    AAAA

                                    _____
                                      Initial

iv. Exercise the Memory function. Store and
    Fetch the following data patterns to
    memory location 0000:

                    0000

                    FFFF

                    5555

                    AAAA

    Verify the data returned is the same as
    data entered.

Witnessed by:
                                    _____
Customer Representative _____ Initial

Raytheon QA Representative _____

Date _____

I-6

Store i the following set of data patterns
to memory, starting at memory location 0000:

0000

0001

0002

0003

0004

0005

0006

0007

Fetch i the entered data starting from
memory location 0000. Verify that data
returned from memory is the same as data
entered to memory.

_____
Initial

v. Exercise the STEP/HALT and RUN functions.
Use the LCP to enter the following simple
Load programs into memory, starting at
location 0000.

Address	Contents	Program
0000	108C	LDS A P*
0001	5555	DC '5555
0002	86FD	JMP-2

Initialize register PR to 0000 and register
ACR to AAAA, using the LCP, and depress the
RESET button. Perform the STEP/HALT func-
tion such that one instruction execution is
performed (two pushbutton depressions).
Verify that the PR register contains 0002,
the ACR register contains 5555, and that
the AR register contains FFFD. Perform the
RUN function. Perform the HALT function.
Observe that the LCP Run light if off.
Verify that the PR and AR registers contain
one of the following two sets of data:

PR	AR
0000	FF4C

or

0002	FFFD

Enter the following simple Store program
into memory, starting at location 0000.

Address	Contents	Program
0000	008C	STS A P*
0001	5555	DC '5555
0002	86FD	JMP-2

Initialize register PR to 0000 and register
ACR to AAAA, and depress the RESET button.
Perform the STEP/HALT function such that
one instruction execution is performed
(two pushbutton depressions). Verify
that the PR register contains 0002 and
that memory location 0001 contains AAAA.

                                                    Initial

2.2   MASTER BUS MODULE TESTS

2.2.1 Master Processor Self-Test

(a) Requirements- Test all Master Processor microinstructions
and microprogram branches that implement
the processor instruction set and depend
only on program execution from a zero-origined
4K memory. Additionally list instruction
functions using a pseudo-random sample of
data word values.

(b) Conditions - Basic test configuration.

(c) Measurement - Enter 0080 into memory locations 0080 and
0081. Initialize register PR to 0100 and
depress the RESET button. Perform the RUN
function. The LCP RUN light shall come on
for a period of approximately 15 seconds.
After the RUN light has gone off, examine
memory locations 0080 and 0081 and verify
that they contain the following information.

Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

                                                    Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.2.2 Master Bus Memory Test

(a) Requirements — Test Master Bus memory via pattern and address tests.

(b) Conditions — Basic test configuration

(c) Measurement — Enter the starting address of the memory sector to be tested into memory location 0080 and the ending address of the sector into location 0081. Initialize register PR to 0600 and depress the RESET button. Perform the RUN function. The LCP RUN light will come on for a period proportional to the size of the tested memory sector (~7 sec. for each 4K block). After the RUN light has gone off, examine memory locations 0080 and 0081 and verify that they contain the following information.

Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

_____
Initial

Execute the Master Bus memory test for the following memory sectors:

From Starting Address	to Ending Address
2000	6FFF
8000	9FFF
C000	CFFF

_____
Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.2.3 Master Bus PIN/RTC Module Test

(a) Requirements – Test the Master Bus Processor's ability with respect to the PIN/RTC to:

(i) Read and write various data patterns to the Mask Register.

(ii) Read RTC counter and verify that it is cleared.

(iii) Read Interrupt Status Register and verify that it is cleared.

(b) Conditions – Basic test configuration

(c) Measurement – Load the PIN/RTC test program into the SSC or SDC. Transfer the contents of the 4K memory, origin C000, to the 4K memory, origin 2000 using the MOVE routine. Enter 0080 into memory locations 0080 and 0081. Initialize register PR to 2000 and depress the RESET button. Place the DC/INRUPTS switch on the TFU into the DC position. Perform the RUN function, which will cause the processor to run for a fraction of a second. Examine memory locations 0080 and 0081 and verify that they contain the following information:

Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

_____
Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.2.4 Master Bus DSIØ Module Test

(a) Requirements – Test the Master Bus Processor's ability
with respect to the DSIØ to:

    (i) Read the Status Word and verify
         that it is cleared.

    (ii) Read Mask bits and verify that they
          are cleared.

    (iii) Write and Read Mask bits.

    (iv) Transmit and receive serial data
          and check status information for
          various control word patterns.

(b) Conditions – Basic test configuration, except that the
procedure is to be repeated four times,
with the SIØ bus cable (SC plug end)
connected to a different SC connector
jack for each test pass. These are:

Test Pass	SC Jack Connection
1	J1
2	J2
3	J3
4	J4

(c) Measurement – Load the DSIØ test program into the SSC or
SDC. Transfer the contents of the 4K memory,
origin C000, to the 4K memory, origin 2000,
using the MOVE routine. For each pass, enter
the address of the SIØ channel to be tested
in memory locations 0080 and 0081. Initialize
register PR to 2002 and depress the RESET button.
Perform the RUN function, which will cause the
processor to run for 5 seconds. Examine memory
locations 0080 and 0081 and verify that they
contain the following information:

Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.2.4   Master Bus DSIØ Module Test (Continued)

(c)   Measurement (Continued)

Also verify at the completion of each pass
that the RCV BUFFER FULL light on the Test
Function Unit is on. Depress the front panel
RESET pushbutton and verify that the SIØ CLR
light comes on and the RCV BUFFER FULL light
goes off at the Test Function Unit.

SIØ channel addresses for each pass are
as follows:

Test Pass	Channel Address
1	FC00
2	FC04
3	FC08
4	FC0C

_____
Initial

2.2.5   Master Bus SCM Test

(a)   Requirements -

(i)   Read Breakpoint Status and verify
that it is cleared.

(ii)   Read Watchdog Timer Status and
verify that it is cleared.

(iii)   Test Breakpoint Register for Break-
point Halt operation.

(iv)   Test ROM and auto-start features.

(v)   Test Watchdog Timer.

(vi)   Test Master Bus Clear distribution.

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

I-12

2.2.5 Master Bus SCM Test (Continued)

(b) Conditions - Basic test configuration.(but without SCM bootstrap PROMS)

(c) Measurement - Load the SCM test into the SSC or SDC. Transfer the contents of the 4K memory, origin C000, to the 4K memory, origin 2000, using the MOVE routine. Enter 0080 into memory locations 0080 and 0081. Initialize Register PR to 2004 and depress the RESET button. Perform the RUN function, which will cause the processor to run for several seconds.

Depress the RELOAD button on the TFU. Examine memory locations 0080 and 0081 and verify that they contain the following information:

Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

                                                 Initial

2.2.6 Master Bus LD/LR Test

(a) Requirements -

     (i) Verify the POWERFAIL function.

     (ii) Verify the SKIP function.

(b) Condition - Basic test configuration.

(c) Measurement - Remove power from the SC. Verify that the POWERFAIL light on the TFU is on. Apply power to the SC. Verify that the SCPWR FAIL light is off. Depress and release the front panel RESET pushbutton.

Using the LCP, enter the following simple program into memory.

Location	Contents	Code
C000	104C	LDS A(P*)
C001	0000	0000
C002	86FD	JMP-2
C003	B800	HALT

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

*CAUTION: This test may alter the contents of the 4K RAM located in the SSC or SDC due to power down/up transients.

Initialize register PR to C000 and depress the
RESET button. Perform the RUN function, putting
the processor in the program loop. Depress the
DC SKIP pushbutton on the TFU. Verify that the
processor halts with the PR register equal to
C004.

Initial

2.3 SLAVE BUS 1 MODULE TESTS

2.3.1 Slave Processor 1 Self Test

(a) Requirements - Test all Slave 1 Processor microinstruc-
tions and microprogram branches that im-
plement the processor instruction set
and depend only on program execution from
a zero origined 4K memory. Additionally,
test instruction functions using a pseudo-
random sample of data word values.

(b) Conditions - Basic test configuration.

(c) Measurement - Transfer the contents of the 4K PROM/RAM,
origin 0000, to the 4K memory, origin 2000,
via the MOVE utility program.

Enter 2080 into memory locations 2080 and
2081, and 0100 into memory location
2000. Depress the RESET button. Store to memory
locations FFC1 and FCCB in sequence with the LCP
to start the Slave 1 processor. After approxi-
mately 15 seconds, examine memory location 2080
and 2081 with the LCP and verify that they con-
tain the following information.

Memory Location	Contents	Meaning
2080	0000	Halt Code
2081	0000	Success Code

Witnessed by: Initial

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.3.2 Slave Bus 1 Memory Test

(a) <u>Requirements</u> - Test all Slave 1 Bus Memory via pattern and address tests.

(b) <u>Conditions</u> - Basic test configuration

(c) <u>Measurement</u> - Transfer the contents of the 4K PROM/ RAM, origin 0000, to the 4K memory, origin 2000, via the MOVE utility program.

Enter the starting address of the Slave 1 memory sector to be tested into memory location 2080 and the ending address of the sector into location 2081. Enter 0600 into memory location 2000. Depress the RESET button. Store to memory locations FFC1 and FFCB in sequence with the LCP to start the Slave 1 processor. Allowing for 7 seconds of execution for each 4K of memory, examine memory locations 2080 and 2081 and verify that they contain the following information:

Memory Location	Contents	Meaning
2080	0000	Halt Code
2081	0000	Success Code

Execute the Slave 1 Bus memory test for the following memory sectors.

From Starting Address	to Ending Address
1000	4FFF
6000	7FFF
C000	C3FF

_____
Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.3.3 Slave Bus 1 PIN/RTC Module Test

(a) Requirements – Test the Master Bus Processor's ability with respect to the PIN/RTC to:

  (i) Read and write various data patterns to the Mask Register.

  (ii) Read RTC counter and verify that it is cleared.

  (iii) Read Interrupt Status Register and verify that it is cleared.

(b) Conditions – Basic test configuration.

(c) Measurement – Load the PIN/RTC test program into the SSC or SDC. Transfer the contents of the 4K RAM, origin C000, to the 4K memory sector origin 4000, via the MOVE utility program.

Enter 2080 into memory locations 2080 and 2081, and 2000 into location 2000. Depress the RESET button. Store to memory locations FFC1 and FFCB in sequence with the LCP to start the Slave 1 processor. Examine memory locations 2080 and 2081 with the LCP and verify that they contain the following information:

2080	0000	Halt Code
2081	0000	Success Code

Initial _____

2.3.4 Slave Bus 1 DSIØ Module Test

(a) Requirements – Test the Master Bus Processor's ability with respect to the DSIØ to:

  (i) Read the Status Word and verify that it is cleared.

  (ii) Read Mask bits and verify that they are cleared.

  (iii) Write and Read Mask bits.

  (iv) Transmit and receive serial data and check status information for various control word patterns.

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

2.3.4 Slave Bus 1 DSIØ Module Test (Continued)

(b) Conditions – Basic test configuration, except that the
procedure is to be repeated twice, with
the SIØ bus cable (SC plug end) connected
to a different SC connector jack for each
test pass. These are:

Test Pass	SC Jack Connections
1	J5
2	J6

(c) Measurement – Load the DSIO Test Program into the SSC or
SDC. Transfer the contents of the 4K RAM,
origin C000, to the 4K memory sector
origin 4000, via the MOVE utility program.
For each pass, enter the SIØ channel
address into memory locations 2080
and 2081, and 2002 into location 2000.
Depress the RESET button. Store to memory
locations FFC1 and FFCB in sequence with the
LCP to start the Slave 1 processor. After
5 seconds, examine memory locations 2080
and 2081 and verify that they contain the
following information:

Memory Location	Contents	Meaning
2080	0000	Halt Code
2081	0000	Success Code

Also verify, after completion of each
pass, that the RCV BUFFER FULL light on
the TFU is on. Depress the front panel
RESET pushbutton and verify that the
SIØCLR light comes on and the RCV BUFFER
FULL light goes off at the TFU.

SIØ channel addresses for each pass are
as follows:

Test Pass	Channel Address
1	FC00
2	FC04

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

Initial _____

I-17

2.4   SLAVE BUS 2 MODULE TESTS

2.4.1   Slave Processor 2 Self Test

(a)   Requirements - Test all Slave 2 processor microinstruc-
                     tions and microprogram branches that im-
                     plement the processor instruction set and
                     depend only on program execution from a
                     zero origined 4K memory. Additionally,
                     test instruction functions using a pseudo-
                     random sample of data word values.

(b)   Conditions -   Basic test configuration

(c)   Measurement - Transfer the contents of the 4K PROM/RAM,
                     origin 0000, to the 4K memory, origin 8000,
                     via the MOVE utility program. Depress the
                     RESET button.

                     Enter 8080 into memory locations 8080
                     and 8081, and 0100 into memory location
                     8000.   Store to memory location
                     FFD1 and FFDB in sequence with the LCP
                     to start the Slave 2 processor. After
                     approximately 15 seconds, examine memory
                     location 8080 and 8081 with the LCP and
                     verify that they contain the following
                     information.

Memory Location	Contents	Meaning
8080	0000	Halt Code
8081	0000	Success Code

                                        _____
                                        Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

I-18

2.4.2 Slave Bus 2 Memory Test

(a) Requirements - Test all Slave 2 Bus Memory via pattern
                    and address tests.

(b) Conditions -   Basic test configuration

(c) Measurement - Transfer the contents of the 4K PROM/RAM
                    origin 0000, to the 4K memory,
                    origin 8000, via the MOVE utility
                    program.

                    Enter the starting address of the Slave 2
                    memory sector to be tested into memory
                    location 8080 and the ending address of
                    the sector into location 8081. Enter
                    0600 into memory location 8000. Depress
                    the RESET button. Store to memory loca-
                    tions FFD1 and FFDB in sequence with the
                    LCP to start the Slave 2 processor.
                    Allowing for 7 seconds of execution for
                    each 4K of memory, examine memory loca-
                    tions 8080 and 8081 and verify that
                    they contain the following information:

Memory Location	Contents	Meaning
8080	0000	Halt Code
8081	0000	Success Code

Execute the Slave 2 bus memory test for
the following memory sectors.

From Starting Address	to Ending Address
1000	1FFF
6000	7FFF
C000	C3FF

                                              _____
                                                 Initial

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

I-19

2.5 BUS TESTS

2.5.1 Master Bus Test

(a) Requirements – Test the following low level interrupts:

Hung Bus Detector (1)
Internal Interrupt Generator (1)
SIØ (4)
LD/LR (7)

(b) Condition   – Basic test configuration

(c) Measurement – Load the Master Bus Test program into the
SSC or SDC. Transfer the contents of the
4K memory, origin C000, to the 4K memory,
origin 2000, using the MOVE routine. Using
the LCP, enter 0080 into memory locations
0080 and 0081. Initialize register PR to
2006 and depress the RESET button. Place
the DC/INRUPTS switch of the TFU in the
INRUPTS position. Perform the RUN func-
tion. Verify that the RUN light on the
LCP goes off and that memory contains
the following information:

Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

Place the DC/INRUPTS switch back into the DC
position.

Initial

2.5.2 Slave Bus 1 Test

(a) Requirements –

(i) Test the SS connector port by controlling
the SS Supervisor Processor, and by re-
sponding to MSG and POWERFAIL interrupts
from the SS.

(ii) Test the following low level interrupts:

Hung Bus Detector (1)
SIØ (2)

(iii) Test Master Clear distribution.

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

I-20

2.5.2 Slave Bus 1 Test (Continued)

(b) Conditions – Basic test configuration

(c) Measurement – Load the Slave 1 Bus Test program into the SSC or SDC. Transfer the contents of the 4K memory, origin C000, to the 4K memory, origin 4000, via the MOVE utility program. Enter 2080 into memory location 2080 and 2081. Enter 200A into memory location 2000. Depress the RESET button. Store 0's to FCF1 before running slave processor 1. Store to memory location FFC1 and FFCB in sequence with the LCP to start the Slave 1 processor. Turn the SS power supply off, then on. Examine memory locations 2080 and verify that they contain the following information:

Memory Location	Contents	Meaning
2080	0000	Halt Code
2081	0000	Success Code

_____
Initial

2.5.3 Slave Bus 2 Test

(a) Requirements –

(i) Write and read data patterns in each of the 16 CAM/RAM control memory locations. Verify operation of the Aux. Buffer Full Interrupt.

(ii) Verify operation of the Aux. Hung Bus Detector interrupt function.

(iii) Test Master Clear distribution.

(b) Condition – Basic test configuration

(c) Measurements – Load the Slave 2 Bus Test program into the SCC or SDC. Transfer the contents of the 4K memory, origin C000, to the 4K memory, origin A000, via the MOVE utility program. Enter 8080 into memory location 8080 and 8081. Depress the RESET button. Enter 1008 into memory location 8000. Store to memory location FFD1 and FFDB in sequence with the LCP to start the Slave 1 Processor. After 5 seconds, examine memory locations 8080 and 8081 and verify that they contain the following information:

Witnessed by:

Customer Representative _____

Raytheon QA Representative _____

Date _____

I-21

Memory Location	Contents	Meaning
8080	0000	Halt Code
8081	0000	Success Code

2.6 System Test

Initial
_____

(a) Requirements – (i) Verify control of the Slave processors by the Master processor, including Control Interface, high level interrupts from Master to Slaves, and low level interrupts from Slaves to Masters.

(ii) Verify generation of synchronized Real Time Clock of Master and Slave 1 processors, including Master control of Slave RTC and Internal Interrupt Generation for Slave 1 processor.

(iii) Verify communication of Slave 1 and Slave 2 processors through the common two port memories.

(iv) Test the Aux. Bus connector port in conjunction with SS connector port stimulation.

(v) Verify the auto-start feature.

(b) Condition – Basic test configuration (with SCM bootstrap test PROMs.

(c) Measurement – Load the SC system test program into the SSC or SDC. Load the tape containing the SS operational software on the device assigned to BIN2. Start the SSC at location 8100. Using the LCP store 0080 into locations 0080 and 0081. Depress the RESET button. Start the SC at location C102. When the RUN light goes out, examine memory locations 0080 and 0081 for the following data:

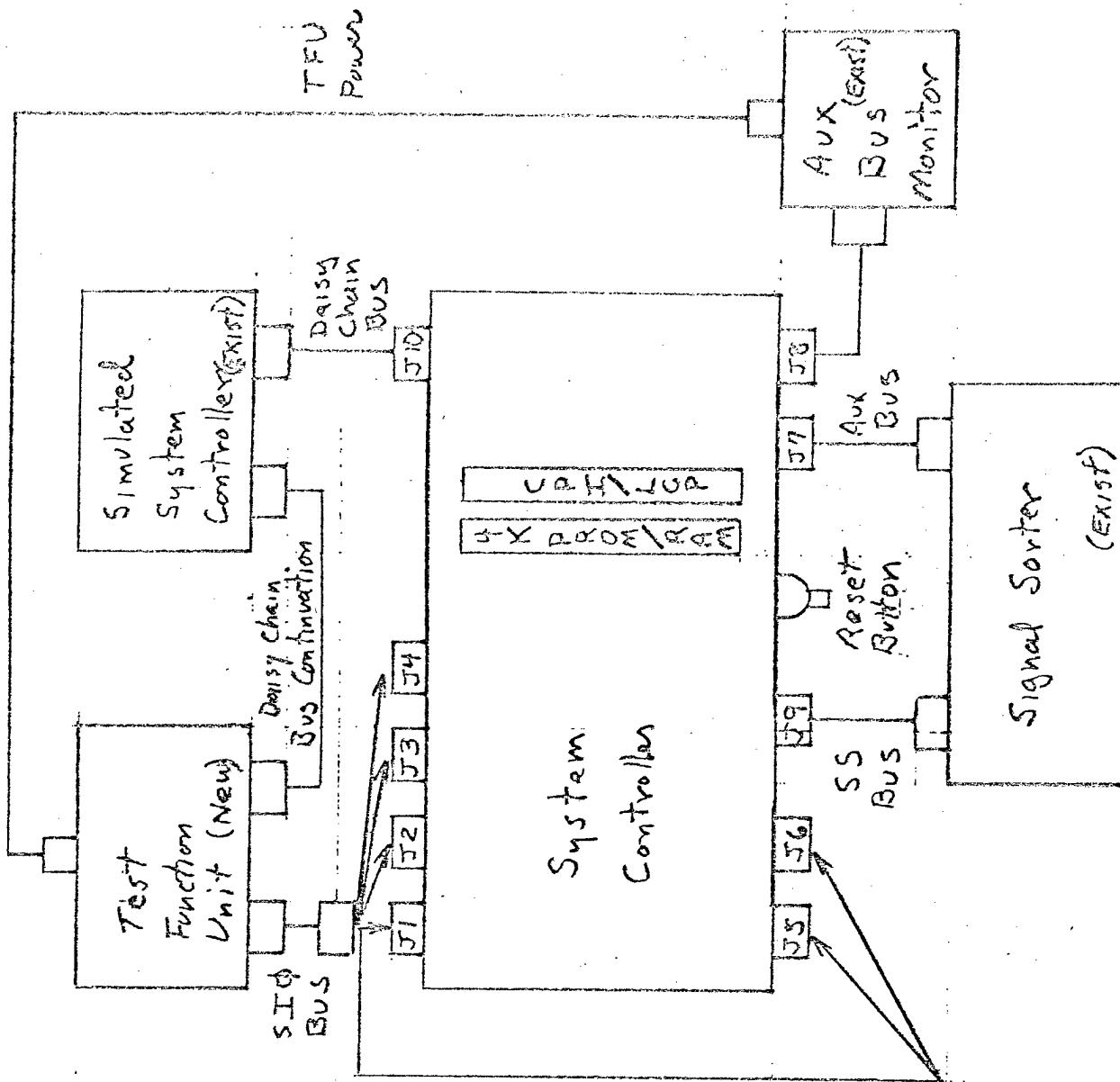| Memory Location	Contents	Meaning
0080	0000	Halt Code
0081	0000	Success Code

– Turn power off for (5) seconds, then turn power on and, when the RUN light goes out after about (15) seconds, confirm that the Master Processor P register contains FF04.

Witnessed by:

Customer Representative:

_____

Raytheon QA Representative:

_____

Date:

I-22

APPENDIX **A**

BASIC TEST EQUIPMENT CONFIGURATION

System Controller Test Configuration

Diagram labels (as handwritten):

- TFU Power
- Aux Bus Monitor (Exist)
- Simulated System Controller (Exist)
- Daisy Chain Bus
- Test Function Unit (New)
- Daisy Chain Bus Continuation
- J10
- J7
- Aux Bus
- SIO Bus
- J1 J2 J3 J4
- J5 J6
- J8
- J9
- SS Bus
- System Controller
- VP H\JUA
- J-Y DROE\RAB
- Reset Button
- Signal Sorter (Exist)

APPENDIX B

TEST PROGRAMS

5413:IEWS:76:69	RP-16 CP Test - PROM Version
5413:IEWS:76:70	Memory Test - PROM Version
5413:IEWS:76:71	IEWS SC Test
	PIN/RTC Test
	SIØ Test
	SCM Test
	Master Bus Test
	SP1 Bus Test
	SP2 Bus Test
5413:IEWS:76:72	IEWS SC System Test

APPENDIX C

OPERATING PROCEDURE FOR MOVE ROUTINE

1. Enter the origin of the 4K memory module, which the program is to be moved FROM, into the XR Register.

2. Enter the origin of the 4K memory module, which the program is to be moved TO, into the BR Register.

3. Enter 05E0 into the PR Register, and depress the RESET button.

4. Put the RP-16 into RUN mode.

APPENDIX D

OPERATING PROCEDURE FOR THE SSC

1. Load the operating system into the SSC and start it.

2. Mount the tape containing the program to be loaded onto Magnetic Tape Drive 0.

3. Type the following commands on the INFOTON keyboard:

```
AS   BIN1, MT0
AS   BIN2, MT1
RW   BIN1
BI   8000
LO
```

To start a program in the SSC, type the command:

```
GO   address
```